A 128 point amplitude-frequency histogram algorithm for real-time EEG amalysis

There is a real need for a method of analyzing EEG in real time which yields as much information as possible with minimal hardware and software expense. The hardware and the algorithm described here was being developed in an effort to distinguish EEG correlates of various psychological events. The hardware and the algorithm described here was being developed in an effort to distinguish EEG correlates of various psychological events. The hardware and the distinguish designed with neurological pathology in mind.

FFT, for Fast Fourier Transform, is presently the most popular algorithm for computer analysis of EEG (along with its mathematical relatives of auto-and cross-correlation). One of the most commonly used outputs from an FFT program is the EEG power spectrum.

The FFT power spectrum suffers from several disadvantages when it is used to investigate psychological events in real time. Perhaps the most serious disadvantage is that the epoch length for FFT must be fixed before data analysis begins. It is not practical to vary the epoch length as data is collected. Since psychological events are of varying and unpredictable duration, this fixed epoch length usually means that the epoch often overlaps into times when the event under study is not occurring.

The second disadvantage of FFT is that it is necessary to give up resolution and accuracy if short epochagere desired. Since many psychological events are of short duration, this can be a major drawback.

The third disadavntage of FFT is that a moderate power signal at a particular frequency which persists throughout the epoch yields a peak in the power spectrum very similar to that produced by a short duration high power signal at that frequency. This disadvantage can be overcome to some extent by shortening the epoch length, but then resolution and accuracy suffer.

The fourth disadmentage of FFT is that the algorithm requires considerable CPU (central prosessing unit) time to run. Because it is a slow running program, many computers are limited to calculating FFT for only one or two channels of EEG at a time. This may mean that several computers could be required to handle 8 channels of EEG in real time. To overcome most of these limitations, I KMMMXM am developing a new algorithm and associated hardware based on period—amplitude analysis.

Period-amplitude analysis has been used from time to time over the years as an off-line technique of EEG analysis. In the last five years or so it has become popular as a real-time EEG analysis technique for biofeedback purposes. I designed a period-amplitude analyzer for Aquarius Electronics five years ago which is still typical of the technique popular today. Describing this instrument will probably make it easier to explain the 128 point histogram system now under development.

As with all EEG systems, the Model 1001A brainwave analyzer begins with an amplifier which accepts the weak signals from the scalp electrodes and amplifies them and seperates them from interfering signals such as 60 Hz power line hum. The amplified EEG signal is of the order of 1 volt in amplitude. This signal them passes through a zero-crossing detector.

The purpose of a zero-crossing detector is to identify the beginning and end of each cycle of the EEG signal. The beginning of a cycle is defined, for these purposes, as being the point when the EEG voltage is zero and rising. The end of that cycle is then the point when the voltage is again zero and rising. In between the beginning and the end of the cycle is an intermediate zero-crossing at which the voltage is falling. In a full wave major period analyzer, these negative-going zero-crossings are ignored.

It should be noted that the EEG signal does not remain at zero voltage for extended periods of time. Even in the absence of any cortical electrical activity, an EEG amplifier will pick up thermal noise from the resistance of the electrode contact with the scalp and this noise will produce continuous tiny fluctuations in the amplifier's output voltage (noise).

The brainwave analyzer measures the period of time between alternate zero-crossings. This is called the full wave major period. It is inversely related to the dominant frequency of the EEG signal. The analyzer compares this period to three adjustable fixed limits and sorts the cycle into a frequency category as a result of this comparison. The Model 1001A limits are set to sort EEG into beta, alpha, theta and delta:

- 13 Hz limit = $\frac{1}{13}$ = 76.9 milliseconds
- 8 Hz limit = 1/8 = 125 milliseconds
- 4 Hz limit = 1/4 = 250 milliseconds

Any EEG cycle shorter than 76.9 milliseconds gets sorted into the beta category, any cycle lasting between 76.9 and 125 ms goes into alpha, any between 125 and 250 are theta and those which last over 250 ms are delta.

The analyzer also compares the peak-to-peak amplitude of each cycle to two adjustable limits. If a cycle is very weak and fails to exceed the lower amplitude limit, the results of the period measurement are ignored. Instead of being sorted into a frequency category, the cycle is sorted into a category set aside for very weak signals, one called "noise." If the cycle is high in amplitude and it exceeds the maximum amplitude limit, then the results of the period analysis are ignored and the cycle is sorted into a category called "artefact."

Thus six categories are defined and each cycle of the EEG signal ends up in one of these six categories, depending on its amplitude and frequency. Feedback tones, visual displays, etc. are controlled from these category outputs. The feedback is essentially real-time since each cycle is analyzed as soon as it is completed.

The disadvantage of this technique of EEG analysis is that only the dominant frequency is detected at any instant. This means that if weak beta is a riding on top of strong alpha, for much of the time the instrument will indicate the presence of only alpha.

This is not as serious a problem as it appears at first glance. A mixture of weak beta and strong alpha will be analyzed as many alpha cycles and a few beta cycles with the proportions roughly correct, considering the relative amplitudes of the two signals. This is because occasionally the weak beta cycle will happen close to the zero-crossing of the stronger alpha cycle and thus produce a secondary zer-crossing of its wwn.

A more serious problem is mimimized aliesing and frequency jitter. The secondary zero crossings of beta on top of alpha will shift the wavelength of the alpha to broaden the spectral peak of the alpha frequency. If the beta causes only a single secondary zero-crossing it can makes cause aliasing so that a new frequency component makes of wavelength equal to ½ the alpha plus ½ the beta is produced.

The aliasing problem can be eliminated by using a bi-directional zero-crossing detector so that $\frac{1}{2}$ closes are enalyzed instead of full cycles. This is what is done in the 128 point histogram system now under development.

Even with its weaknesses, full wave period analysis correlates well with FFT. Beatty, J. and Figueros, C. Behavior Research Methods and Instrumentation 6: 293-295 (1794) compared this kind of period-measuring EEG analysis with FFT for 1.024 second epochs and fount that it correlated fairly well - the largest errors being in the beta category. When they tried period-amplitude analysis (where each cycle is weighted according to Its amplitude on being sorted into a category) the correlation was even better - between 0.79 and 0.81. This correlation is high enough to indicate that period-amplitude analysis can be a usable alternative to FFT, especially in situations where FFT is at a disadvantage, such as the real time detection of psychological events.

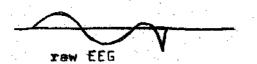
The algorithm now under development is a logical extension of the technique used in the brainwave apalyzer described above. As it now stands, the program sorts each cycle of the EEG signal into one of 128 categories. These categories are defined by frequency (period) and amplitude limits. There are sixteen frequency categories and might eight amplitude sub-categories in each frequency category. Thus the results of the computer analysis area an 8 x 16 matrix. Each number in the matrix is the number of EEG ½ cycles which feel inside a particular set of amplitude—frequency limits.

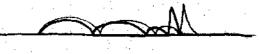
The system under development will eventually be an 8 channel system which will analyze 8 EEG signals in real time. The prototype which is now being tested is a siggle channel system. It is more economical to experiment with only one channel until the algorithm is more or less finalized. Although the single channel system is somewhat different than the proposed 8 channel system, it merits description here and will help clarify the later description of the 8 channel system.

The EEG amplifier used in the single channel system is battery operated. This eliminates electrical shock hazard and minimizes 60 Hz hum pick-up. The EEG signal from the amplifier passes through an optical isolator. This device converts the electrical signal of varying voltage into a light of varying brightness. The light them shines onto a phototransistor which converts the light signal back into an electrical signal, which is them further amplified and filtered.

The block diagram on the next page may help you follow the process from here. We are at point "B". Now the EEG signal is sent in two directions. In one direction it passes through a zero-crossing detector. In the single channel system, this detector only looks for positive-going zero-crossings and outputs a narrow pulse at each. This pulse exits at point "e" on the diagram by going to the computer's interrupt request line. This interrupt request stops the computer from executing the main program and causes it to service the interrupt, in this case it causes it to imput data from the cycle of EEG just completed.

The other branch of the output from the optical isolator goes to a precision rectifier. This takes the absolute value of the EEG signal, ie, it makes the signal always positive by reflecting negative helf-cycles around the voltage axis. A diagram below makes this clearer.





rectified EEG

The rectified EEG signal is then sent to a peak-holding A/D converter. This circuit digitizes the peak amplitude of the signal and holds the value as an 8 bit binary number until it is reset. This 8 bit resolution allows amplitudes from 0 to 255 microvolts to be measured with 1 microvolt resolution. The gain of the EEG amplifier is adjusted to get this scale factor.

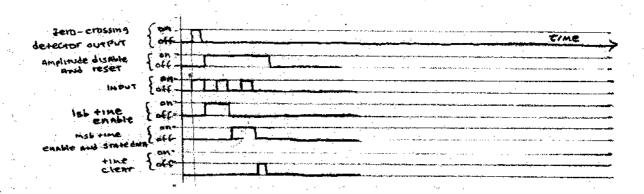
The eight output bits from the A/D converter are triestate logic which allows them to be connected onto a party-line type that bus leading to the computer's input port. Data from the A/D converter appears on the data bus only when the A/D converter data output is enabled. The same data bus is shared by other parts of the system. Only one part of the system at a time sends data onto the data bus while all of the others are disconnected by being disabled.

The next part of the system is the timer which measured the duration of each cycle. It is a counter which is counting a 1 kHz clock. The timer has 12 hits of resolution. This means that it measures time from 0. 4.095 seconds in 1/1000 of a second.

The timer is actually made up of three 4 bit counters which are cascaded. Since the computer system handles 8 bit words, all 12 bits of time data can't be input in a single word. The least significant 8 bits form one word of data which can be put onto the bus by enabling it. The most significant 4 bits of the time data form half of another data word whach can be put on the data bus.

The other half of that third word of data is four bits of experimental data which can be used to tell the computer about experimental conditions which might affect or correlate with EEG. In the experiments which are planned these bits will be used to indicate the psychological state of the person whose EEG is being analyzed. A four bit block of data allows for 16 possible states.

A timing diagram, below, shows the usual sequence of events at the end of a cycle of the EEG signal.



Normally, amplitude data is on the data bus. This data will not necessarily be valid until the very end of the cycle, so the computer ignores it until the zero-crossing detector signals the end of a cycle. Then the amplitude data on the bus is input by the computer. Once amplitude has been stored in memory, the amplitude word is disabled. The same signal also resets the amplitude A/D converter so that it can begin to track and hold the peak amplitude of the next cycle of the EEG signal.

This whole process is set in motion by an interrupt request which is triggered by the end of cycle pulse from the zero-crossing detector. The interrupt causes the computer to stop executing the main program and collect the data which is waiting.

Once the amplitude data has been input, the least significant bits of time are enabled, input and stored in memory. Finally the four most significant bits of time data are enabled along with the four bits of psychological state data, these data are input and stored.

Omce all of the data for a cycle has been input, amplitude is enabled once more, thus allowing the amplitude A/D converter to begin tracking the new cycle. The timer is reset and allowed to begin timing the new cycle.

The flow chart on the next page makes the sequence of events from here on in a bit clearer. In this primative system, for test purposes, the epoch length has been fixed. The duration of each cycle is added to a total which is then compared to the fixed epoch length. If the end of the epoch has been reached a flag h is set and data begins accumulating in a new area of memory in the computer so that the epoch just completed can be printed out.

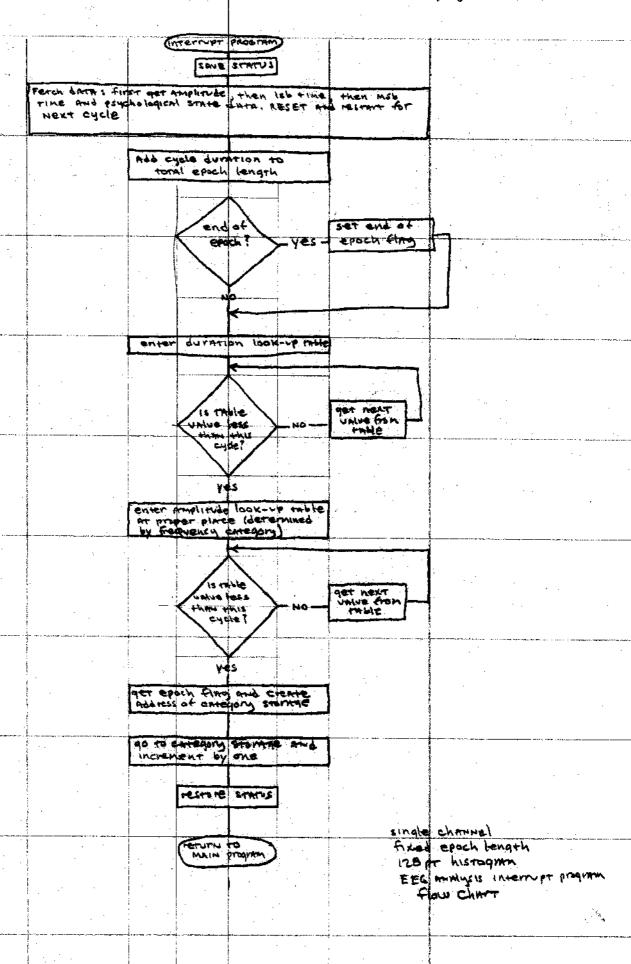
The duration of the cycle is next compared to the duration limits which define the 16 frequency categories. These limits are stored in a look-up table. Once the computer has found the proper frequency category, it leaves the first look-up table and enters a second table to check the amplitude of the cycle against the limits defining the 8 amplitude categories.

EEG amplifiers are imperfect in that they respond unequally to different EEG frequencies. The amount of sensitivity variation with frequency is an importent EEG amplifier specification. The amplifier's sensitivity is always deliberately reduced for very high and very low frequency signals to minimize noise and artefacts. There is usually a pertion of the frequency range, in the middle of the amplifier's passband, in which the amplifiers responds equally to different frequencies.

For most accurate analysis of EEG it is desirable to compensate for variations in the amplifier's frequency response. The program does this by having 16 sets of amplitude limits, one set for each of the 16 frequency categories it sorts brainwaves into. Thus, the amplifier's limits for an extreme high frequency category, for example, can be adjusted to compensate for the amplifier's reduced sensitivity.

To test this system of compensation, an amplifter with mederately mearrow flat frequency response area in mid-band was used for the prototype system. The table below shows the amplitude limits used for each frequency category.

128-up	64-128	32-64	16-32	8-16	4-8	2-4	02	<u>.</u> .	octal duration
32	16	8	A	2	· 1	0	0	0+4 Hz	372
67	34	17	8	4	2	4	8	4-5	310
106	53	27	\$3	7	3	2	D	5-6	247
128	64	32	16	5-8-4	4	2	0	6-7	217
128	64	32	16	8	4	2	Ð	7₩8	175
116	58	29	15	8	4	2	Ð	8 - 9	157
106	53	27	13	7	3	2	Ð	9-10	144
99	49	23	12	6	3	2	Ø	10-11	133
85	43	21	4.5		3	e si 📫 e	0	11-12	123
75	38	19	B	4	2	1	9	12-13	115
67	34	17	8	4	2	4	Ø	13-14	107
58	29	15	7	4	2	•	0	14⊷15	077
32	16	6	4	2	4	0=	O	16-18	070
27	- 13	7	4	2	4	0	- O	18-20	062
22	11	5	3	1	Ü	.0	8	20-22	056
11	5	3	1	0	O	0	Ü	22 ⇔ up	000



Once the proper amplitude sub-category within the frequency category has been located, the computer checks the epoch flag and selects the proper memory location. The number at that location is incremented by one to count the present cycle.

The analysis of the cycle is now completer, the program restores status and returns control to the main program so that it can pick up where it was interrupted.

The main program is the routine which the computer executes between interrupts (see flow cahrt on page 16). This program has to clear out all of the data storage areas before the start of the first epoch. In the prototype system it also prints out a heading to explain all later print out of data. Then the program waits for a signal (a buttonpush) to start the first epoch. Once the epoch is started, the computer loops looking for an end-of-epoch flag. This is the signal for the computer to begin printing out the completed epoch's data. The epoch number is printed at the head of each block of data. Once the data is all printed, the epoch number is incremented by one and the data storage just printed is cleared out for the next epoch.

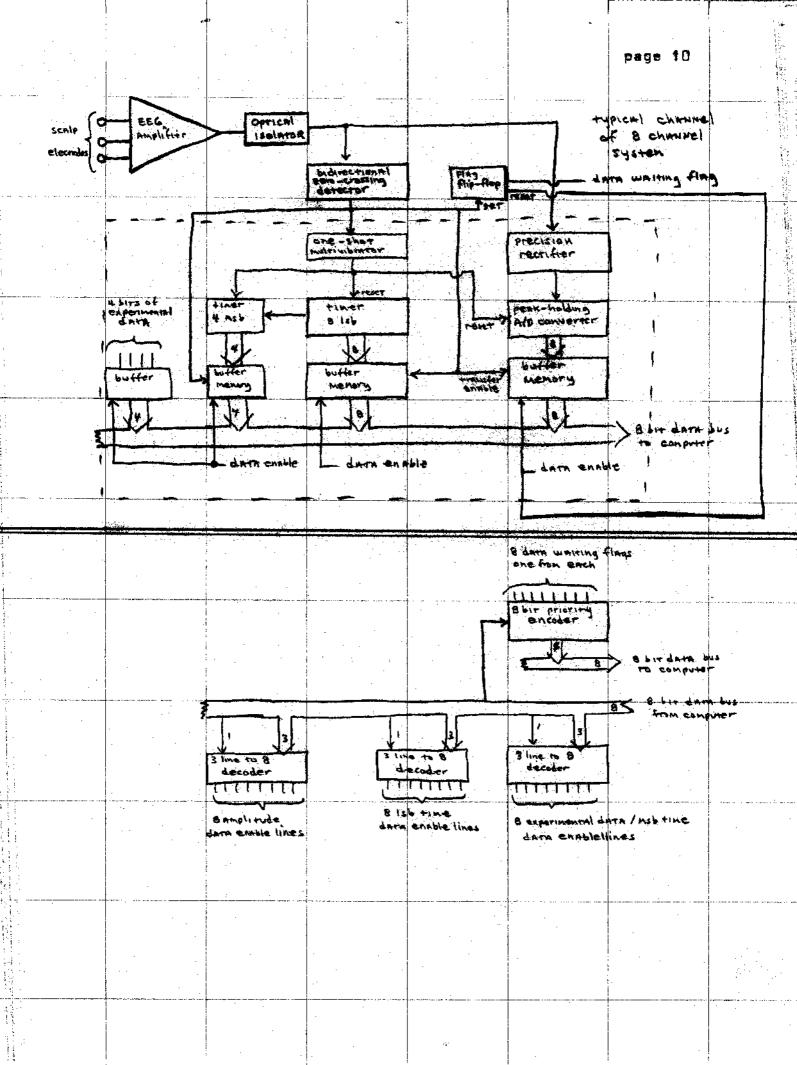
While one data storage area is printing, the other is collecting data. Thus there is one area where data from even numbered epochs accumulates and a second area where odd numbered epochs are stored. This way no data is lost.

This output format is very crude and has been used in initial tests because it is very easy to program. In a system intended for practical use the data would be printed out with more complete headings, with leading zeros suppressed and would probably be supplemented by a graph which would provide an isometric view of the three dimensional histogram formed by the data. Such a graph would be easier to interpret at a glance than a table of numbers while the table would be more useful for statistical calculations.

Once testing of the prototype system is completed, the construction of a more elaborate system will begin. This will be an 8 channel system in contrast to the single channel prototype. As a result of testing the prototype, several changes in design have been made in plans for the 8 channel system.

There will be 8 EEG amplifiers, all with fairly broad flat frequency response, all battery powered. These amplifiers will be optically isolated and the isolated outputs will drive 8 zero-crossing detectors. These zero-crossing detectors will differ from the prototype in that every zero-crossing will be detected instead of alternate zero-crossings. Thus the system will analyze each 1 cycle of the EEG signal instead of full cycles (to eliminate aliasing).

The block diagram on the next page (top) shows one typical chamnel of eight chamnels. The area inside the dotted line is the circuitry contained on a single plugain printed circuit board whose design has been completed. Eight of these boards will be used in the completed system.



Many changes have been made in the 8 channel system hardware, some to increase accuracy and others to minimize the workload on the computer, in the interests of maximizing speed. In the single channel system the computer took care of housekeeping such as resetting the timer and A/B converter. In the eight channel system the hardware resets itself at the end of each cycle. The single channel system is interrupt driven, the eight mix channel system may be also, or it may be polled, depending on which turns out to be easiest to run.

When a half-cycle of the EEG ends in one channel, that biddirectional zero-crossing detector sends out a pulse. This pulse goes to the transfer enable input of three buffer memories, thus storing the valid amplitude and time data. The same pulse also sets a flag flip flop which will remember and signal that data is waiting in that channel. In an interrupt drivin system the flag would trigger an interrupt. The flag will remain set until the data has been picked up by the computer. The buffer memories and automatic resetting ability of this circuit gives the computer time to do other jobs before coming to pick up the data waiting for it. The zero-crossing detector's output elso triggers a one shot multivibrator which generates the reset pulse for the timer and A/D converter right after the data transfer to the buffer memories has been completed.

The diagram at the bottom of page 10 shows how the 8 channels are linked togther. Each channel of EEG has a flag bit which is set if data is waiting to be picked up. A priority encoder creates a four bit word from these flag bits. The words is all ones if no data is waiting, if data is waiting, the word is the address of the highest priority channel with data waiting. The computer can check this word from time to time to poll or it can be interrupted if the word is not all ones.

A single 8 bit output word is used to control the appearance of all data on the single 8 bit input bus. The three least significant bits of this word are the channel number. The more significant bits indicate what data from that channel are to be put on the data bus: amplitude, lsb time, or msb time and psychological state data.

If there is spare CPU time after handling all 8 channels of EEG the system may grow to include other physiological measures such as BSR/GSR. In the planned series of experiments there will be three states of consciousness which observers will be looking for. An area of computer memory will be set aside for each of these three states and a fourth area for all EEG not falling into one of these states. Each of the 128 amplitude/frequency categories for a particular EEG channel, for a particular paychological state, during a particular epoch (bynthe same even/odd system used in the single channel system)will be assigned two words in the computer memory. These two 8 bit words will allow up to 65,000 cycles to be counted before memory overflows.

A flow chart of the EEG input subroutine to be used with this system appears on the next page. This subroutine may be called at least as often as twice the highest EEG frequency, or it may become an interrupt handling program. If the program is called and no data is waiting, control is rapidly returned to the calling program. If data is waiting, the EEG input routing loop repeatedly and checks the priority encoder's output after it has completed picking up data, to be sure more data isn't maiting. After all data has been paicked up, control is returned to the main program.

The data will occupy 16k words of memory, 6k for the current epoch and 8k for the epoch being cutput. Data will be output onto magnetic tape in digital form so that it can be put back into the computer later for statistical analysis. It will take about 2 minutes to dump 6k onto tape, and this period of time will probably determine the epoch length in the first series of experiments. As soon as one epoch has been output, the next epoch will begin outputting. Each block of data will be identified as to EEG channel, consciousness category and epoch number. In the experiments planned, the data will be put back into the computer later so that templete patterns of EEG for each consciousness category can be built up and tested statistically.

Pages 14 and 15 pare sample output from the single channel 128 point histogram program in its most primative form. One page is a couple of epoch of occipital frontal EEG with eyes open, the other page is with eyes closed.

The eight amplitude categories are spread out on the horazontal axis. The first category on the left-hand side of the page at the top is 0-4 Hz with amplitude above 128 microvolts (peak). The number in that position is the number of cycles which occurred during that epoch which fell inside the amplitude and frequency limits.

Further development of this system will happen in the next few months.

September, 1976

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UP-128- 64- 32- 16- 8 - 4 - 2
      0-4.
      4-5. 128 POINT EEG HISTOGRAM
      5-6. HORIZONTAL AXIS IS AMPLITUDE
      6-7. IN MICROVOLTS
      7-8. VERTICAL AXIS IS FREQUENCY
      8-9.
           IN HERTZ
     9-10-
    10-11. EACH POINT IS NUMBER OF
    11-12. CYCLES INSIDE LIMITS
    12-13.
    13-14. EPOCH IS 1 MINUTE
    14-16.
    16-18. PUSH * TO START 1ST EPOCH
    18-20.
   20-22.
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  4-5. 128 POINT EEG HISTOGRAM
   5-6. HORIZONTAL AXIS IS AMPLITUDE
   6-7. IN MICROVOLTS
  7-8. VERTICAL AXIS IS FREQUENCY
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10-11. EACH POINT IS NUMBER OF
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12-13.
13-14. EPOCH IS 1 MINUTE
14-16-
16-18. PUSH * TO START 1ST EPOCH
18-20.
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page

(Program reset all converter + timer clear storage frens of memory Print Hending push 765 STAT ALD CONVENTER And timer enable interrupt epoch ? print spoch # Print data from epoch Add 1 to clemout stomage just

Single channel
fixed epoch
main program